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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,764	11/25/2003	Masashi Yonemaru	829-618	3114

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NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

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06/22/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/720,764	YONEMARU, MASASHI	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-23* is/are pending in the application.

4a) Of the above claim(s) *2,3,5,7 and 9-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 10/17/2006 has been entered.

Applicant's Pre-Brief Conference request has been considered and the Committee has found Applicant's argument's persuasive. Essentially, Applicant argued that the new claim limitations "(a) the first and second PMOS transistors are connected directly in series, and/or (b) the first and second NMOS transistors are connected directly in series," are minimally disclosed by "the instant specification as originally filed, at least via the figures thereof."

The additional limitations are not particularly complicated, and therefore need no complex explanation. The Examiner was in error to not view the originally filed application, including the original drawings, from the point of view of one of skill in the art at the time of filing. Recently found evidence makes it clear that, at the time of filing, one of skill in the art would have been completely familiar with the concept of the additional limitation the figures convey in their minimal way. For example, figure 5 and column 7 lines 32-37 of Varma 6,794,916 show applicant's new limitation in the context of a useful device. Varma explains (emphasis added):

> FIG. 5 derives a static flip-flop 500 from the design in FIG. 4A by substituting the series inverter/pass transistor combination 440, 440' with **WELL-KNOWN** 4-transistor CMOS clocked phase inverters 540, 540'. Since the clocked inverter circuit 540, 540' is a one-stage circuit compared to the two-staged series combination in FIG. 4A, the speed of the flip-flop 500 in FIG. 5 is higher.

The Examiner's error was in not recognizing that Applicant's figures were merely intended to minimally convey to Applicant's readers a concept already made crystal-clear by Varma, as well as the others, prior to Varma, to whom Varma refers with his characterization of the additionally claimed circuit as "well-known."

2. Finality of the action mailed 11/08/2006 is withdrawn. This action is responsive to substantial amendments to the claims filed 10/17/2006 (amendments made in response to a first action on the merits) and is made final for that reason.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by ROBINSON ET AL. (20050182809).

Robinson et al. discloses a semiconductor integrated circuit, comprising a first cell 62 comprising a plurality of transistors; a second cell 66 comprising a PMOS transistor section 72-74, the PMOS transistor section 72-74 comprising a first PMOS transistor 72 and a second PMOS transistor 74 connected to the first PMOS transistor 72 in series, and an NMOS transistor section 76-78, the NMOS transistor section 76-78 comprising a first NMOS transistor 76 and a second NMOS transistor 78 connected to the first NMOS transistor 76 in series, wherein a predetermined scheme is used to connect between the first cell 62 and the second cell 66, between the plurality of transistors in the first cell 62, and between the PMOS transistor section 72-74 and the NMOS transistor section 76-78 in the second cell 66, wherein the first cell 62 functions as a logic operation (barrel-shifting) circuit for outputting data; and the second cell 66 functions as a driver circuit (by way of feedback or "pull-up" transistor 79) for driving the logic operation circuit and as a data retaining circuit ("dynamic latch," note paragraphs 0050-0052) for retaining data output by the logic operation (barrel-shifting) circuit, and wherein the first PMOS transistor 72, the second PMOS transistor 74, the first NMOS transistor 76, and the second NMOS transistor 78 each comprise a gate, a source, and a drain; a first source voltage is applied to the source of the first PMOS transistor 72; a second source voltage is applied to the source of the first NMOS transistor 76; one of the gate of the first PMOS transistor 72 and the gate of the second PMOS transistor 74 is connected to an

input terminal IN, an input signal being input to the input terminal IN, and the other is connected to a first gate control signal input terminal ϕ (clock signal), a first gate control signal being input to the first gate control signal input terminal ϕ ; one of the gate of the first NMOS transistor 76 and the gate of the second NMOS transistor 78 is connected to the input terminal IN, and the other is connected to a second gate control signal input terminal ϕ-BAR (inverse clock signal), a second gate control signal being input to the second gate control signal input terminal ϕ-BAR; and the drain of the second PMOS transistor 74 and the drain of the second NMOS transistor 78 are connected to an output terminal OUT. Note figures 8, 9, and paragraphs 0049-0055 of Robinson et al.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over ROBINSON ET AL. (20050182809) in view of Murakami (5,457,723).

Robinson et al. discloses a semiconductor integrated circuit having every limitation of claim 6 except the limitation that the first cell must include a P-MOS transistor and an N-MOS transistor. Note figures 8, 9, and paragraphs 0049-0055 of Robinson et al.

However, Murakami discloses a semiconductor integrated circuit with a first cell identical in form and function (barrel shifter) to Robinson et al.'s (barrel shifter) first cell, except Murakami's first cell barrel shifter includes a P-MOS transistor P31 and an N-MOS transistor N31. Note figures 4 and 5 and column 4 lines 16-22 of Murakami. Murakami explains that "the barrel shifter having the circuit of CMOS structure described at column 4 lines 16-22 and shown in FIG. 4 and FIG. 5 requires no circuit for loading the initial data and has such an ideal advantage of reducing electric consumption as that it is operable from high frequency to clock stop condition. This is extremely advantageous for so-called lap top type or palm top type microcomputers which operate primarily from a battery." It would therefore have been obvious to a person having skill in the art to modify Robinson et al.'s semiconductor integrated circuit by including the P-MOS and N-MOS transistors in the first cell, such as taught by Murakami), in order to avoid requiring a circuit for loading the initial data to thus reduce current consumption as would prove advantageous in battery operation.

Response to Arguments

5. Applicant's arguments with respect to claims 1,6, and 8 successfully overcome the case for rejection made in the Final Rejection (now withdrawn) mailed 11/08/2006 but are moot in view of the new ground(s) of rejection.

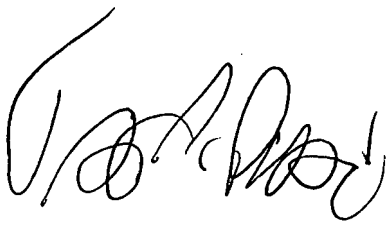
Conclusion

6. Applicant's amendment, filed 10/17/2006, necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L. Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Sue A. Purvis, at 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



/Thomas L. Dickey/
Primary Examiner
Art Unit 2826